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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/656,550 | 09/06/2000 | William A Chren, Jr. | 00-LM-007 | 9623 |

30428 7590 07/02/2003

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| EXAMINER |
|---|
| WHITTINGTON, ANTHONY T |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/656,550 | CHREN, JR., WILLIAM A | |
| | Examiner | Art Unit | |
| | Anthony T Whittington | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Claim Objections*

Claims 1-24 are objected to because of the use of the acronyms (i.e. RNS and OHRNS). The Examiner would appreciate if the Applicant would express these acronyms in full, unabbreviated form. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7,10-15 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chren, Jr.(U.S. 5,430,764) in view of Arkin (U.S. 5,917,834).

As per claims 1 and 10, Chren, Jr. substantially teaches an arithmetic circuit and digital signal processing device for use with an RNS comprising all the elements of the instant application. Chren, Jr. teaches an arithmetic core (A/U, 121) for performing an RNS arithmetic

operation in Figure 3. Chren, Jr. does not explicitly disclose test circuitry for inducing oscillation at the output of the arithmetic core and logic circuitry producing a passed/fail signal.

However Arkin, an analogous art, teaches test circuitry (10) for inducing oscillation at the output of the arithmetic core and logic circuitry (98) producing a passed/fail signal in Figure 1 and 5.Arkin refers in greater detail to Figure 1 and Figure 5 in column 2, lines 59-68 and column 7, lines 21-65. The fact that the arithmetic core, test circuitry and logic circuitry are coupled together in certain configuration has no significance in terms of patentability in accordance with the MPEP 2144.04(V).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Chren, Jr.'s system by combining Arkin's test circuitry and logic circuitry with Chren, Jr.'s system. This modification would have been obvious to a person having ordinary skill in the art because a person having ordinary skill in the art would have been motivated to use the RNS implementation with the test circuitry to reduce pipeline stage delays and latches for shorter test time and less circuitry in testing circuits, as suggested by Chren, Jr.in column 3, line 66 through column 4, line 7.

As per claims 2 and 11, Chren, Jr. substantially teaches an arithmetic circuit and digital signal processing device for use with an RNS comprising all the elements of the instant application. Chren, Jr. teaches an arithmetic core (A/U, 121) for performing an RNS arithmetic operation in Figure 3. Chren, Jr. does not explicitly disclose a counter and a comparator.

However Arkin, an analogous art, teaches counter (120) for counting the oscillations at the output of the arithmetic core and comparator (74) for comparing the passed/fail signal in

Figure 3 and 6. The fact that the counter and comparator are coupled in certain configuration has no significance in terms of patentability in accordance with the MPEP 2144.04(V).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Chren, Jr.'s system by combining Arkin's test circuitry and logic circuitry with Chren, Jr.'s system. This modification would have been obvious to a person having ordinary skill in the art because a person having ordinary skill in the art would have been motivated to use the RNS implementation with the test circuitry to reduce pipeline stage delays and latches for shorter test time and less circuitry in testing circuits, as suggested by Chren, Jr. in column 3, line 66 through column 4, line 7.

As per claims 3-7, 12-15 and 20-22, Chren, Jr. substantially teaches an arithmetic circuit and digital signal processing device for use with an RNS comprising all the elements of the instant application. Chren, Jr. teaches an arithmetic core (A/U, 121) for performing an RNS arithmetic operation in Figure 3. Chren, Jr. teaches a plurality of isolation buffers(122) in Figure 8. Chren, Jr. does not explicitly disclose transmission gates and a controller.

However Arkin, an analogous art, teaches transmission gates and a controller in Figure 4.Arkin refers to Figure 4 in column 6, lines 35-67.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Chren, Jr.'s system by combining Arkin's test circuitry and logic circuitry with Chren, Jr.'s system. This modification would have been obvious to a person having ordinary skill in the art because a person having ordinary skill in the art would have been motivated to use the RNS implementation with the test circuitry to reduce pipeline

stage delays and latches for shorter test time and less circuitry in testing circuits, as suggested by Chren, Jr.in column 3, line 66 through column 4, line 7.

As per claims 18, Chren, Jr. substantially teaches a method for use with an RNS arithmetic circuit comprising all the elements of the instant application. Chren, Jr. teaches an arithmetic core (A/U, 121) for feeding the output of the arithmetic core back to one of its inputs in Figure 3. Chren, Jr. does not explicitly disclose test circuitry for inducing oscillation at the output of the arithmetic core and logic circuitry for producing a passed/fail signal.

However Arkin, an analogous art, teaches test circuitry (10) for inducing oscillation at the output of the arithmetic core and logic circuitry (98) for producing a passed/fail signal in Figure 1 and 5.Arkin refers in greater detail to Figure 1 and Figure 5 in column 2, lines 59-68 and column 7, lines 21-65.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Chren, Jr.'s system by combining Arkin's test circuitry and logic circuitry with Chren, Jr.'s system. This modification would have been obvious to a person having ordinary skill in the art because a person having ordinary skill in the art would have been motivated to use the RNS implementation with the test circuitry to reduce pipeline stage delays and latches for shorter test time and less circuitry in testing circuits, as suggested by Chren, Jr.in column 3, line 66 through column 4, line 7.

As per claim19, Chren, Jr. substantially teaches an arithmetic circuit and digital signal processing device for use with an RNS comprising all the elements of the instant application. Chren, Jr. teaches an arithmetic core (A/U, 121) for performing an RNS arithmetic operation in Figure 3. Chren, Jr. does not explicitly disclose a counter and a comparator.

However Arkin, an analogous art, teaches counter (120) for counting the oscillations at the output of the arithmetic core and comparator (74) for comparing a passed/fail signal in Figure 3 and 6.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Chren, Jr.'s system by combining Arkin's test circuitry and logic circuitry with Chren, Jr.'s system. This modification would have been obvious to a person having ordinary skill in the art because a person having ordinary skill in the art would have been motivated to use the RNS implementation with the test circuitry to reduce pipeline stage delays and latches for shorter test time and less circuitry in testing circuits, as suggested by Chren, Jr. in column 3, line 66 through column 4, line 7.

Claims 8,9,16,17, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chren, Jr.(U.S. 5,430,764) in view of Prior Art Admissions.

As per claims 8,9,16,17, 23 and 24, Chren, Jr. substantially teaches an arithmetic circuit and digital signal processing device for use with an RNS comprising all the elements of the instant application. Chren, Jr. teaches an arithmetic core (A/U, 121) for performing an RNS arithmetic operation in Figure 3. Chren, Jr. does not explicitly disclose OHRNS addition and OHRN multiplication.

However, the Applicant admitted to the features OHRNS addition and OHRN multiplication as prior art on page 6, lines 11-25 of the specification. Prior art admissions can be used as prior art in accordance with MPEP 2129.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Chren, Jr.'s system to use OHRNS operations instead of

normal RNS operations. This modification would have been obvious to a person having ordinary skill in the art because a person having ordinary skill in the art would have been motivated to use the OHRNS implementation for the minimal possible activity factor and low power dissipation, as suggested by the Applicant page 6, lines 19-20 of the specification.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of art with respect to digital process monitoring in general:

U.S. Pat No. 4,949,249 to Wambergue

U.S. Pat No. 5,081,629 to Criswell et al.

U.S. Pat No. 6,509,728 to Uchino et al.

U.S. Pat No. 4,433,413 to Fasang

U.S. Pat No. 4,924,467 to Criswell

U.S. Pat No. 4,996,527 to Houk et al.

U.S. Pat No. 5,249,144 to Falk

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T Whittington whose telephone number is 703-306-5617. The examiner can normally be reached on Monday-Friday 7:30a.m.-4:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

A.W.
June 19, 2003

Guy J. Lamarre
for

**Albert DeCady**
**Primary Examiner**